Opcode						remark	instruction	syntax	
6	5	5	5	5	6				bits
00 0000	0	rt	rd	shamt	0		sll	sll rd, rt, shamt	
00 0000	0	0	0	0	0		nop	nop	
00 0000	rs	cc;0	rd	0	1	cc (3 bits)	movf	movf rd, rs, cc	
00 0000	rs	cc;1	rd	0	1	cc (3 bits)	movt	movt rd, rs, cc	
00 0000	0	rt	rd	shamt	2		srl	srl rd, rt, shamt	
00 0000	0	rt	rd	shamt	3		sra	sra rd, rt, shamt	
00 0000	rs	rt	rd	0	4		sllv	sllv rd, rt, rs	
00 0000	rs	rt	rd	0	6		srlv	srlv rd, rt, rs	
00 0000	rs	rt	rd	0	7		srav	srav rd, rt, rs	
00 0000	rs	0	0	0	8		jr	jr rs	
00 0000	rs	0	rd	0	9		jalr	jalr rs, rd	
00 0000	0	0	rd	0	0x10		mfhi	mfhi rd	
00 0000	rs	0	0	0	0x11		mthi	mthi rs	
00 0000	0	0	rd	0	0x12		mfl	mfl rd	
00 0000	rs	0	0	0	0x13		mli	mli rs	
00 0000	rs	rt	0	0	0x18		mult	mult rs, rt	
00 0000	rs	rt	0	0	0x19		multu	multu rs, rt	
00 0000	rs	rt	0	0	0x1a		div	div rs, rt	
00 0000	rs	rt	0	0	0x1b		divu	divu rs, rt	
00 0000	rs	rt	rd	0	0x20		add	add rd, rs, rt	
00 0000	rs	rt	rd	0	0x21		addu	addu rd, rs, rt	
00 0000	rs	rt	rd	0	0x22		sub	sub rd, rs, rt	
00 0000	rs	rt	rd	0	0x23		subu	subu rd, rs, rt	
00 0000	rs	rt	rd	0	0x24		and	and rd, rs, rt	
00 0000	rs	rt	rd	0	0x25		or	or rd, rs, rt	
00 0000	rs	rt	rd	0	0x26		xor	xor rd, rs, rt	
00 0000	rs	rt	rd	0	0x27		nor	nor rd, rs, rt	
00 0000	rs	rt	rd	0	0x2a		slt	slt rd, rs, rt	
00 0000	rs	rt	rd	0	0x2b		sltu	sltu rd, rs, rt	
00 0000	rs	rt	0		0x30		tge	tge rs, rt	
00 0000	rs	rt	0		0x31		tgeu	tgeu rs, rt	
00 0000	rs	rt	0		0x32		tlt	tlt rs, rt	
00 0000	rs	rt	0		0x33		tltu	tltu rs, rt	
00 0000	rs	rt	0		0x34		teq	teq rs, rt	
00 0000	rs	rt	0		0x36		tne	tne rs, rt	
00 0000	rs	rt	rd	0	0xa		movz	movz rd, rs, rt	
00 0000	rs	rt	rd	0	0xb		movn	movn rd, rs, rt	
00 0000	0	0	0	0	0xc		syscall	syscall	
00 0000	code				0xd		break	break code	
00 0001	rs	0	offset				bltz	bltz rs, label	
00 0001	rs	1	offset				bgez	bgez rs, label	
00 0001	rs	8	imm				tgei	tgei rs, imm	
00 0001	rs	9	imm				tgeiu	tgeiu rs, imm	
00 0001	rs	0x10	offset				bltzal	bltzal rs, label	
00 0001	rs	0x11	offset				bgezal	bgezal rs, label	
00 0001	rs	0xa	imm				tlti	tlti rs, imm	
00 0001	rs	0xb	imm				tltiu	tltiu rs, imm	
00 0001	rs	0xc	imm				teqi	teqi rs, imm	
00 0001	rs	0xe	imm				tneqi	tneqi rs, imm	

00 0010	target						j	j target
00 0011	target						jal	jal target
00 0100	rs	rt		offset			beq	beq rs, rt, label
00 0101	rs	rt		offset			bne	bne rs, rt, label
00 0110	5	5	5	5	6	bits		
00 0110	rs	0		offset			blez	blez rs, label
00 0111	rs	0		offset			bgtz	bgtz rs, label
00 1000	rs	rt		imm			addi	addi rt, rs, imm
00 1001	rs	rt		imm			addiu	addiu rt, rs, imm
01 0000	0	rt	rd	0	0		mfc0	mfc0 rt, rd
01 0000	4	rt	rd	0	0		mtc0	mtc0 rd, rt
01 0000	0x10	0	0	0	0x18		eret	eret
01 0001	0	rt	rd	0	0		mfc1	mfc1 rt, rd
01 0001	4	rt	rd	0	0		mtc1	mtc1 rt, rd
01 0001	0x10	ft	fs	fd	0		add.s	add.s fd, fs, ft
01 0001	0x11	ft	fs	fd	0		add.d	add.d fd, fs, ft
01 0001	0x10	ft	fs	fd	1		sub.s	sub.s fd, fs, ft
01 0001	0x11	ft	fs	fd	1		sub.d	sub.d fd, fs, ft
01 0001	0x10	ft	fs	fd	2		mul.s	mul.s fd, fs, ft
01 0001	0x11	ft	fs	fd	2		mul.d	mul.d fd, fs, ft
01 0001	0x10	ft	fs	fd	3		div.s	div.s fd, fs, ft
01 0001	0x11	ft	fs	fd	3		div.d	div.d fd, fs,ft
01 0001	1	0	fs	fd	4		abs.d	abs.d fd, fs
01 0001	0x10	0	fs	fd	4		sqrt.s	sqrt.s fd, fs
01 0001	0x11	0	fs	fd	4		sqrt.d	sqrt.d fd, fs
01 0001	1	0	fs	fd	5		abs.s	abs.s fd, fs
01 0001	0x10	0	fs	fd	6		mov.s	mov.s fd, fs
01 0001	0x11	0	fs	fd	6		mov.d	mov.d fd, fs
01 0001	0x10	0	fs	fd	7		neg.s	neg.s fd, fs
01 0001	0x11	0	fs	fd	7		neg.d	neg.d fd, fs
01 0001	0x10	cc;0	fs	fd	0x11	cc (3 bits)	movf.s	movf.s fd, fs, cc
01 0001	0x10	cc;1	fs	fd	0x11		movt.s	movt.s fd, fs, cc
01 0001	0x11	cc;0	fs	fd	0x11	cc (3 bits)	movf.d	movf.d fd, fs, cc
01 0001	0x11	cc;1	fs	fd	0x11		movt.d	movt.d fd, fs, cc
01 0001	0x10	rt	fs	fd	0x12		movz.s	movz.s fd, fs, rt
01 0001	0x11	rt	fs	fd	0x12		movnzd	movnzd fd, fs, rt
01 0001	0x10	rt	fs	fd	0x13		movn.s	movn.s fd, fs, rt
01 0001	0x11	rt	fs	fd	0x13		movn.d	movn.d fd, fs, rt
01 0001	0x11	0	fs	fd	0x20		cvt.s.d	cvt.s.d fd, fs
01 0001	0x14	0	fs	fd	0x20		cvt.s.w	cvt.s.w fd, fs
01 0001	0x10	0	fs	fd	0x21		cvt.d.s	cvt.d.s fd, fs
01 0001	0x14	0	fs	fd	0x21		cvt.d.w	cvt.d.w fd, fs
01 0001	0x10	0	fs	fd	0x24		cvt.w.s	cvt.w.s fd, fs
01 0001	0x11	0	fs	fd	0x24		cvt.w.d	cvt.w.d fd, fs
01 0001	0x10	0	fs	fd	0xc		round.w.s	round.w.s fd, fs
01 0001	0x11	0	fs	fd	0xc		round.w.d	round.w.d fd, fs
01 0001	0x10	0	fs	fd	0xd		trunc.w.s	trunc.w.s fd, fs
01 0001	0x11	0	fs	fd	0xd		trunc.w.d	trunc.w.d fd, fs
01 0001	0x10	0	fs	fd	0xe		ceil.w.s	ceil.w.s fd, fs
01 0001	0x11	0	fs	fd	0xe		ceil.w.d	ceil.w.d fd, fs
01 0001	0x10	0	fs	fd	0xf		floor.w.s	floor.w.s fd, fs

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01 0001	0x11	0	fs	fd	0xf		floor.w.d	floor.w.d fd, fs
01 0001	0x10	ft	fs	cc;0	fc;0xc	cc (3 bits); fc	c.lt.s	c.lt.s cc, fs, ft
01 0001	0x11	ft	fs	cc;0	fc;0xc	cc (3 bits); fc	c.lt.d	c.lt.d cc, fs, ft
01 0001	0x10	ft	fs	cc;0	fc;0xe	cc (3 bits); fc	c.ls.s	c.le.s cc, fs, ft
01 0001	0x11	ft	fs	cc;0	fc;0xe	cc (3 bits); fc	c.le.d	c.le.d cc, fs, ft
01 0001	0x10	ft	fs	cc;0	fc;2	cc (3 bits); fc	c.e.s	c.e.s cc, fs, ft
01 0001	0x11	ft	fs	cc;0	fc;2	cc (3 bits); fc	c.e.d	c.e.d cc, fs, ft
01 0001	8	cc;0	offset			cc (3 bits)	bc1f	bc1f cc, label
01 0001	8	cc;1	offset			cc (3 bits)	bc1t	bc1t cc, label
01 1100	rs	rt	0	0	0		madd	madd rs, rt
01 1100	rs	rt	0	0	1		maddu	maddu rs, rt
01 1100	rs	rt	rd	0	2		mul	mul rd, rs, rt
01 1100	rs	rt	0	0	4		msub	msub rs, rt
01 1100	rs	rt	0	0	5		msubu	msubu rs, rt
01 1100	rs	0	rd	0	0x20		clz	clz rd, rs
01 1100	rs	0	rd	0	0x21		clo	clo rd, rs
10 0000	rs	rt	offset				lb	lb rt, address
10 0001	rs	rt	offset				lh	lh rt, address
10 0010	rs	rt	offset				lwl	lwl rt, address
10 0011	rs	rt	offset				lw	lw rt, address
10 0100	rs	rt	offset				lbu	lbu rt, address
10 0101	rs	rt	offset				lhu	lhu rt, address
10 0110	rs	rt	offset				lwr	lwr rt, address
10 1000	rs	rt	offset				sb	sb rt, address
10 1001	rs	rt	offset				sh	sh rt, address
10 1010	rs	rt	offset				swl	swl rt, address
10 1011	rs	rt	offset				sw	sw rt, address
10 1110	rs	rt	offset				swr	swr rt, address
11 0000	rs	rt	offset				ll	ll rt, address
11 0001	rs	ft	offset				lwc1	lwc1 ft, address
11 0001	rs	ft	offset				swc1	swc1 ft, address
11 1000	rs	rt	offset				sc	sc rt, address
11 1101	rs	ft	offset				sdc1	sdc1 ft, address
00 1010	rs	rt	imm				slti	slti rt, rs, imm
00 1011	rs	rt	imm				sltiu	sltiu rt, rs, imm
00 1100	rs	rt	imm				andi	andi rt, rs, imm
00 1101	rs	rt	imm				ori	ori rt, rs, imm
00 1110	rs	rt	imm				xori	xori rt, rs, imm
00 1111	0	rt	imm				lui	lui rt, imm

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